

1    **CLAIMS:**

2    What we claim is:

3    1.    A data storage device comprising:

4                an array of resistive memory cells having rows and columns;

5                a set of diodes electrically connected in series to a plurality of memory

6                cells in the array;

7                a plurality of word lines extending along the rows of the array;

8                a plurality of bit lines extending along the columns of the array;

9                a first selected memory cell in the array, wherein the first selected memory

10              cell is positioned between a first word line in the plurality of word lines and a first

11              bit line in the plurality of bit lines; and

12              a circuit electrically connected to the array and capable of monitoring a

13              signal current flowing through the first selected memory cell and comparing the

14              signal current to an average reference current in order to determine which of a first

15              resistance state and a second resistance state the first selected memory cell is in.

16    2.    The device of claim 1, wherein the array of resistive memory cell comprises a

17              magnetic random access memory (MRAM) cell.

18    3.    The device of claim 2, wherein the MRAM memory cell comprises a tunnel

19              junction.

20    4.    The device of claim 1, wherein the set of diodes comprises a thin-film diode.

21    5.    The device of claim 1, further comprising a second selected memory cell in the

22              array, wherein the first selected memory cell is in a first layer of the array and

23              wherein the second selected memory cell is in a second layer of the array.

24    6.    The device of claim 1, wherein the circuit is capable of obtaining the average

25              reference current by placing the first selected memory cell in the first resistance

26              state, sensing a first reference current while the first selected memory cell is in the

27              first resistance state, placing the first selected memory cell in the second

28              resistance state, sensing a second reference current while the first selected

29              memory cell is in the second resistance state, and averaging the first reference

30              current and the second reference current to obtain the average reference current.

31    7.    The device of claim 6, wherein the circuit is capable of returning the first selected

32              memory cell to an original resistance state wherein the first selected memory cell

33              has the signal current flowing there through.

1       8. The device of claim 1, wherein the circuit is capable of obtaining the average  
2       reference current from an externally supplied source.

3       9. The device of claim 1, wherein the circuit is capable of obtaining the average  
4       reference current by monitoring memory cells other than the first selected memory  
5       cell.

6       10. The device of claim 1, wherein the circuit is capable of writing to the first selected  
7       memory cell by applying sufficient energy to the first word line and the first bit  
8       line to transform the first selected memory cell from a first resistance state to a  
9       second resistance state.

10      11. A method of sensing a resistance state of a first selected memory cell in a data  
11       storage device that includes an array of resistive memory cells, a plurality of word  
12       lines extending along rows of the array, a plurality of bit lines extending along  
13       columns of the array, a first selected memory cell in the array, wherein the first  
14       selected memory cell is positioned between a first word line in the plurality of  
15       word lines and a first bit line in the plurality of bit lines, and a circuit electrically  
16       connected to the array, the method comprising:  
17               providing a set of diodes electrically connected in series to a plurality of  
18       memory cells in the array;  
19               sensing a signal current flowing through the first selected memory cell  
20       with the array;  
21               comparing the signal current to an average reference current; and  
22               determining which of a first resistance state and a second resistance state  
23       the first selected memory cell is in by comparing the signal current to the  
24       reference current.

25      12. The method of claim 11, wherein the providing step comprises providing a set of  
26       thin-film diodes.

27      13. The method of claim 11, wherein the sensing step comprises sensing the signal  
28       current flowing through an magnetic random access memory (MRAM) cell.

29      14. The method of claim 11, wherein the sensing step comprises sensing the signal  
30       current flowing through the MRAM memory cell that includes a tunnel junction.

31      15. The method of claim 14, wherein the determining step comprises determining  
32       which of an anti-parallel ferromagnetic state and a parallel ferromagnetic state the  
33       MRAM memory cell is in.

- 1 16. The method of claim 11, further comprising obtaining the average reference  
2 current from an externally supplied source.
- 3 17. The method of claim 11, further comprising obtaining the average reference  
4 current by monitoring cells other than the first selected memory cell.
- 5 18. The method of claim 11, further comprising:
  - 6 placing the first selected memory cell in the first resistance state;
  - 7 sensing a first reference current while the first selected memory cell is in  
8 the first resistance state;
  - 9 placing the first selected memory cell in the second resistance state;
  - 10 sensing a second reference current while the first selected memory cell is in  
11 the second resistance state; and
  - 12 averaging the first reference current and the second reference current to  
13 obtain a value for the average reference current.
- 14 19. The method of claim 18, further comprising returning the first selected memory  
15 cell to the state that the first selected memory cell was in before the first reference  
16 current and the second reference current were sensed.
- 17 20. The method of claim 11, further comprising sensing a signal current flowing  
18 through a second selected memory cell positioned in a different layer of the array  
19 than where the first selected memory cell is positioned.